ORTEC/EG&G TD811 TIME DIGITIZER MANUAL

1. DESCRIPTION

The TD811 Octal Time Digitizer contains eight precision time-to-digital converters that are coupled to a common start input for measuring time intervals over a range of 0 to 200 ns with a resolution of 100 ps.

A valid start is a pulse that is accepted through the Start input when the TD811 is in a reset status. On receipt of a valid start the stop inputs are rapidly enabled and an internal busy latch is set (which may be tested by CAMAC command). Stop signals can be accepted within 200 ns after the valid start and each stop signal signals a normal conversion in its channel.

At the leading edge of the valid start input, eight separate timing capacitors begin to charge with constant current. Each capacitor continues to charge until a stop pulse arrives at its input; then it discharges at a much slower rate. If no stop is furnished within 200 ns, an internal timer simulates a stop and the measurement will be overrange. This limits the converter circuit and reduces recovery time. For each channel in which the stop input was received within the 200-ns time range, the time is converted to a charge; an internal clock is gated to a scaler through both the charge and discharge intervals to accumulate the measurement that is temporarily stored in the scaler.

The Time Digitizer is designed with a 90-μs fixed conversion time, which is independent of the start-to-stop period and provides full LAM logic. At the completion of the conversion cycle, the unit generates a LAM service request by setting a LAM status bit. The LAM may be controlled at the module level by an enable/disable latch and can be tested by CAMAC command in accordance with recommended practice.

If it is desired to abort the conversion cycle, a front panel fast Clear input may be used at any time during the first 70 μs of the 90-μs conversion interval and total reset will be accomplished within 1 μs from the leading edge of the Clear signal. The Time Digitizer is then ready to accept another start signal. After the 70-μs time window has elapsed, the Clear input is blocked and the normal conversion cycle will be completed.

A Veto input is included to achieve fast gating of the start input signal. If veto is used, it must overlap the valid start signal to prevent a response in the TD811.

Each scaler contains 11 valid data bits and a 12th bit that is used to indicate overrun in that section. The scaler capacity, using the 11 valid bits, is 2047 units of time (100 ps/time unit). The accumulated data for each measurement is stored in its register for subsequent readout through the CAMAC Dataway.

The module can be tested externally by use of the common stop input. All eight registers will then contain measurements of the same start-to-stop interval. If computer testing is desired, the module will respond to the CAMAC F(25) command; this furnishes a start input and no stop input so all eight scalers will overrun and set the 12th bit, and the module then generates a request for service.

The TD811 may be blocked by either the internal busy latch or a Dataway inhibit signal. An indicator marked "B" on the front panel lights to show that the input is blocked, and start inputs are rejected.

An indicator marked "N" on the front panel lights to show when the unit is being addressed in the CAMAC system.

2. SPECIFICATIONS

2.1. DATA

Start Input One per module common to all sections; accepts NIM fast negative logic signals $\geq$5 ns (preferably <10 ns); Z_{in} 50Ω, dc coupled; protected to ±5 V dc.

Stop Inputs, 0 to 7 Eight front panel connectors, one per channel; each accepts NIM fast negative logic signals $\leq$5 ns to terminate the time interval for its section; Z_{in} 50Ω, dc coupled; protected to ±5 V.

Common Stop One per module common to all sections for dynamic test function; accepts NIM fast negative logic signals $\geq$5 ns to terminate the time interval for all sections simultaneously; Z_{in} 50Ω, dc coupled; protected to ±5 V; typical timing +5 ns relative to single stop input.

2.2. LOGIC

Veto One front panel connector per module, common to all sections; accepts NIM fast negative logic signals $\geq$5 ns to

block the start input; must overlap start signal; Z_{in} 50Ω, dc coupled; protected to ±5 V; response rise 3 ns and decay 15 ns.

Clear One front panel connector per module, common to all sections; accepts NIM fast negative logic signals ≥5 ns to cancel conversion and reset the unit without LAM; must be furnished <70 μs after valid start; Z_{in} 50Ω, dc coupled; protected to ±5 V.

2.3. OUTPUTS

Data 11 bits per channel onto CAMAC read lines R1 through R11, per TID-25875.

Overflow Indicated by bit onto CAMAC read line R12. Jumper provisions included to furnish this bit onto CAMAC read line R16.

2.4. INDICATORS AND CONTROL

B Indicator lights when module is blocked and cannot accept a start input.

N Indicator lights when module is being addressed in the CAMAC system.

Calibrate Eight internal potentiometers, one per channel, calibrate the effective conversion for each channel.

2.5. PERFORMANCE

Full Scale Time Range 4 to 200 ns, using 11 binary bits.

Calibration 100 ps/bit.

Resolution 100 ps.

Integral Nonlinearity ±0.1% (10% to 100% of full scale).

Differential Nonlinearity ±2% (10% to 100% of full scale).

Conversion Time ~90 μs; all channels in parallel.

Temperature Coefficient ≤±0.02%/°C (0 to 50°C).

2.6. CAMAC CODES

F(0)·A(k) (k = 0 to 7) read selected register.

F(2)·A(k) (k = 0 to 6) read selected register.

F(2)·A(7) Read register 7; clear all registers, busy, and LAM.

F(8)·A(12) Test LAM; Q = LAM.

F(10)·A(12) Clear LAM.

F(11)·A(12) Clear all registers, busy, and LAM.

F(24)·A(12) Disable LAM.

F(25)·A(k) (k = 0 to 7) test all registers. This triggers a simulated start and an overrun stop internally in the module to test response in all sections.

F(26)·A(12) Enable LAM.

F(27)·A(12) Test busy; Q = busy.

C Clears all data registers, busy, and LAM status.

Z Clears all data registers, busy, and LAM status, and disables LAM.

I Inhibits operation of all sections.

Q Returned for all F·A function codes except F(8)·A(12) and F(27)·A(12) where the Q response is conditional.

X Returned for all F·A function codes.

2.7. POWER REQUIRED

Maximum +6 V, 520 mA; −6 V, 720 mA; +24 V, 85 mA; −24 V, 55 mA.